INTEGRATED CIRCUITS

# DATA SHEET

# UAA3500HL
## Pager receiver

Preliminary specification
Supersedes data of 1999 Mar 30
File under Integrated Circuits, IC17

2000 Jan 18

Philips Semiconductors

PHILIPS

## FEATURES

- Double frequency conversion, zero-IF receiver with:
  - Configurable in all paging bands (130 to 930 MHz)
  - Low noise amplifier featured with four step Automatic Gain Control (AGC)
  - Down-conversion mixers
  - On-chip, zero-IF channel filter
  - I/Q, non-demodulated outputs
  - Highpass filters to remove DC offsets.
- External Voltage Controlled Oscillator (VCO):
  - Both Local Oscillators (LOs) derived from the VCO.

## APPLICATIONS

- FLEX$^{TM}$, ERMES and POCSAG pagers
- Remote control terminals.

## GENERAL DESCRIPTION

The UAA3500HL is a one-chip pager receiver complying with POCSAG, FLEX$^{TM}$ and ERMES standards. The IC performs in accordance with specifications in the −10 to +55 °C temperature range.

The UAA3500HL contains a front-end receiver, which can be configured through external components for any frequency band between 130 and 930 MHz. The back-end receiver consists of the channel filter and limiters. An external VCO ensures the Local Oscillator (LO) for the front-end. Designed in an advanced BiCMOS process, it combines high performance with low-power consumption and a high degree of integration, thus reducing external component costs and total radio size.

Its first advantage is to remove the expensive SAW filter necessary in a superhet architecture, replacing it by an integrated, elliptic channel filter that provides 70 dB adjacent channel rejection. The receive front-end section consists of a low-noise amplifier that drives mixers through an external LC image rejection filter. The output drives the I and Q second mixers, whose outputs are at zero frequency. The receiver back-end section consists of filters (channel filtering), limiters (limited output required) and high-pass filters (DC block) to remove DC offsets. Outputs are I and Q, undemodulated signals.

Its second advantage is to provide the two LO signals from one VCO only, tuned by a PLL. An on-chip frequency divider-by-2 and buffers provide the LO sources.

Its third advantage is to provide two voltage regulators, allowing to obtain 1.0 and 1.8 V regulated voltages.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| UAA3500HL | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

### QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS[1] | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$ | supply voltage 1 (B++;see note 2) | | 1.85 | 2.1 | 3.3 | V |
| $V_{CC2}$ | supply voltage 2 (B+; see note 2) | | 1.05 | 1.4 | 1.5 | V |
| $I_{CC1(RX)}$ | supply current from B++ | RX section on; DC tested | | | | |
| | | $f_{RF}$ = 160 MHz | – | 2.4 | – | mA |
| | | $f_{RF}$ = 280 MHz | – | 2.4 | – | mA |
| | | $f_{RF}$ = 930 MHz | 2.35 | 2.7 | 3 | mA |
| $I_{CC2(RX)}$ | supply current from B+ | RX section on; DC tested | | | | |
| | | $f_{RF}$ = 160 MHz | – | 1.3 | – | mA |
| | | $f_{RF}$ = 280 MHz | – | 1.4 | – | mA |
| | | $f_{RF}$ = 930 MHz | 1.85 | 2.3 | 2.45 | mA |
| $NF_{RX}$ | receiver noise figure | from RF input to 2nd mixer input | | | | |
| | | $f_{RF}$ = 160 MHz | – | 2.7 | – | dB |
| | | $f_{RF}$ = 280 MHz | – | 3.1 | – | dB |
| | | $f_{RF}$ = 930 MHz | – | 4.4 | – | dB |
| $P_{i(ref)}$ | RF input sensitivity | 3% BER | | | | |
| | | $f_{RF}$ = 160 MHz; 1600 bits/s 2-level FSK | – | –128.5 | – | dBm |
| | | $f_{RF}$ = 280 MHz; 1600 bits/s 2-level FSK | – | –128 | – | dBm |
| | | $f_{RF}$ = 930 MHz; 6400 bits/s 2-level FSK | – | –126.5 | – | dBm |
| | | $f_{RF}$ = 930 MHz; 6400 bits/s 4-level FSK | – | –123 | – | dBm |
| ACR | adjacent channel rejection | | 65 | 70 | – | dB |
| $T_{amb}$ | ambient temperature | | –10 | +25 | +55 | °C |

**Notes**

1. For 930 MHz band; for other conditions see Chapters “DC characteristics” and “AC characteristics”.
2. For B+ and B++, see Fig.3.

## BLOCK DIAGRAM

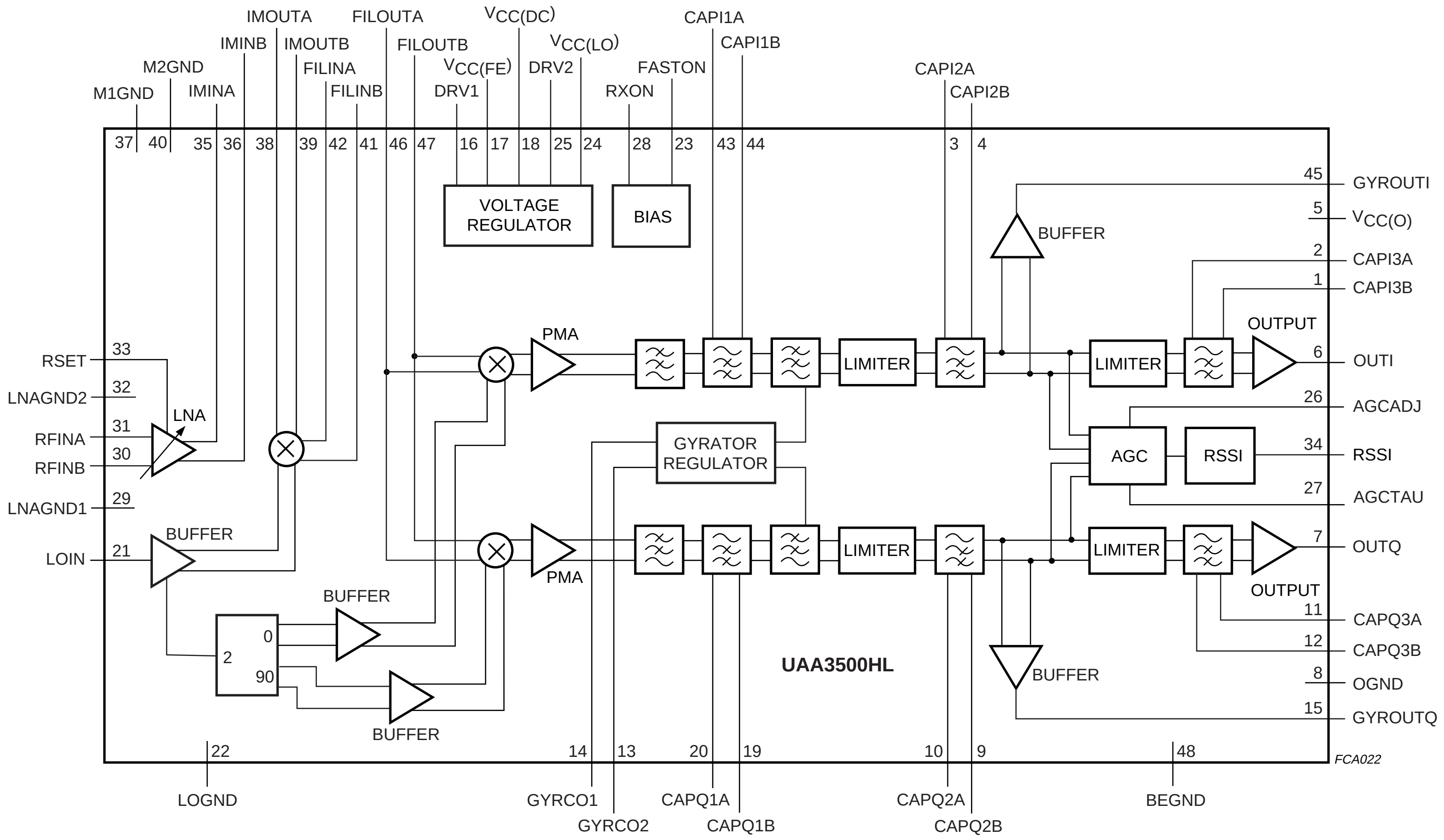



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| CAPI3B | 1 | 3rd DC filter (I path) external capacitor B (I path) |
| CAPI3A | 2 | 3rd DC filter (I path) external capacitor A (I path) |
| CAPI2A | 3 | 2nd DC filter (I path) external capacitor A (I path) |
| CAPI2B | 4 | 2nd DC filter (I path) external capacitor A (I path) |
| $V_{CC(O)}$ | 5 | output stage supply voltage B++ (I path) |
| OUTI | 6 | output I and Q signals (I path) |
| OUTQ | 7 | output I and Q signals (Q path) |
| OGND | 8 | output stage ground |
| CAPQ2B | 9 | 2nd DC filter external capacitor B (Q path) |
| CAPQ2A | 10 | 2nd DC filter external capacitor A (Q path) |
| CAPQ3A | 11 | 3rd DC filter external capacitor A (Q path) |
| CAPQ3B | 12 | 3rd DC filter external capacitor B (Q path) |
| GYRCO2 | 13 | external resistor to set-up gyrator filter cut-off frequency |
| GYRCO1 | 14 | external resistor to set-up gyrator filter cut-off frequency |
| GYROUTQ | 15 | Q-gyrator output |
| DRV1 | 16 | regulator driver (1.8 V) |
| $V_{CC(FE)}$ | 17 | regulated voltage for front-end (1.8 V) |
| $V_{CC(DC)}$ | 18 | input voltage from DC-to-DC converter (2.1 V) |
| CAPQ1B | 19 | 1st DC filter external capacitor (Q path) |
| CAPQ1A | 20 | 1st DC filter external capacitor (Q path) |
| LOIN | 21 | LO input |
| LOGND | 22 | LO strip ground |
| FASTON | 23 | fast mode enable |
| $V_{CC(LO)}$ | 24 | regulated voltage for LO strip (1.0 V) |
| DRV2 | 25 | regulator driver (1.0) |
| AGCADJ | 26 | AGC loop gain control |
| AGCTAU | 27 | AGC loop time constant |
| RXON | 28 | receiver mode enable |
| LNAGND1 | 29 | receiver LNA (Low Noise Amplifier) ground 1 |
| RFINB | 30 | LNA input B |
| RFINA | 31 | LNA input A |
| LNAGND2 | 32 | receiver LNA ground 2 |
| RSET | 33 | LNA current setup |
| RSSI | 34 | received signal strength indicator |
| IMINA | 35 | image rejection filter input A |
| IMINB | 36 | image rejection filter input B |
| M1GND | 37 | first mixer ground |
| IMOUTA | 38 | image rejection filter output A |
| IMOUTB | 39 | image rejection filter output B |
| M2GND | 40 | second mixers ground |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| FILINB | 41 | band filter input B |
| FILINA | 42 | band filter input A |
| CAPI1A | 43 | 1st DC filter external capacitor (I path) |
| CAPI1B | 44 | 1st DC filter external capacitor (I path) |
| GYROUTI | 45 | I-gyrator output |
| FILOUTA | 46 | band filter output to second mixers |
| FILOUTB | 47 | band filter output to second mixers |
| BEGND | 48 | receiver back-end ground |

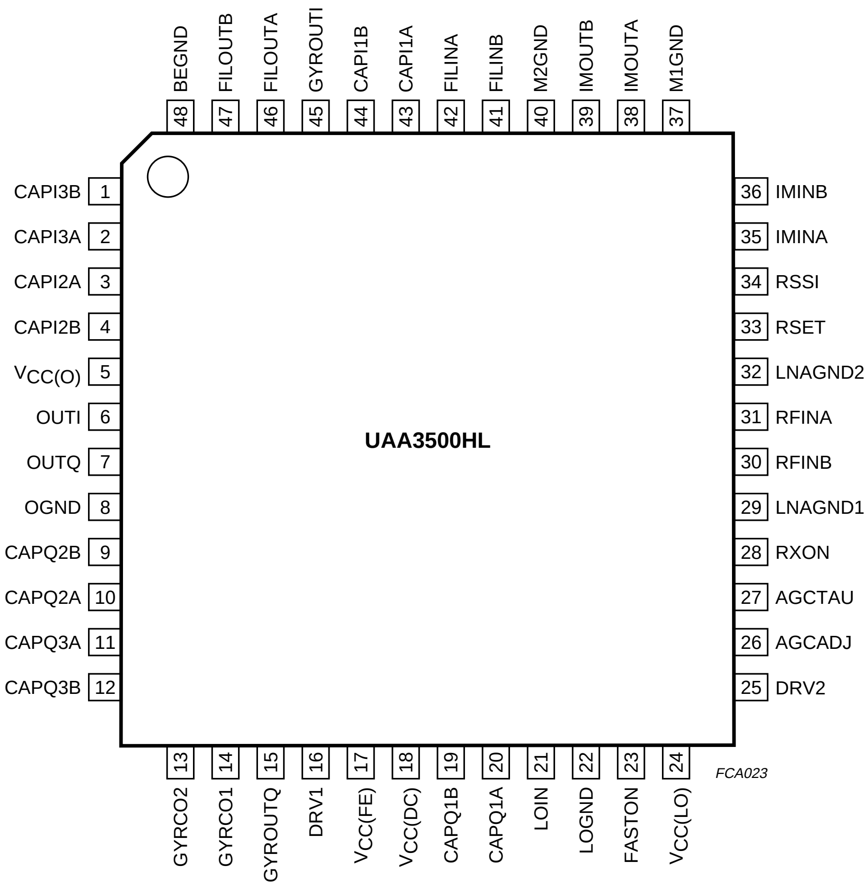



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

### Receiver front-end section

The receiver front-end consists of an LNA, followed by the first and the second mixers. For operation at low frequency (160 and 280 MHz, for instance), the first mixer can be bypassed, saving some current. The image rejection is done by an external LC filter placed between the LNA, the first mixer and the antenna selectivity. The IF band is filtered by an external filter placed between the first mixer and the second mixers for the I and Q paths. The RF signals are in phase, and the LO signals are shifted by 90°. The output signals are at zero frequency.

To increase the immunity to interferers, an AGC loop controls the LNA gain by attenuating the RF input signal. Four steps of attenuation are possible (each having 8 dB), ranging therefore from 0 to 32 dB. The AGC loop threshold level and time constant may be controlled externally at pins AGCADJ and AGCTAU. The second LO I/Q phase shift is made by a quadrature divider, whose input is the VCO oscillating signal.

The LNA current is setup by an external resistor. All the receivers (front-end and back-end) are turned on by pin RXON.

### Receiver back-end section

The down-converted signal is amplified and then filtered by a Sallen-Key filter, which shows a notch at 15 kHz and about 6 dB rejection out-of-band. Then comes the first high-pass filter (DC block), followed by the gyrator filter, which performs an elliptic, 7-pole low-pass filtering. The signal is then amplified by the first limiter, filtered by the second DC block, amplified again, and filtered again by the third DC block. Finally, an output stage delivers the signal with rail-to-rail logic levels.

The first, second and third DC block frequencies are set at 4, 8 and 12 Hz respectively by external 330 nF capacitors.

The two voltage regulators are also activated by RXON.

At the output of the gyrator filter, the signal is buffered and logarithmically converted. It then controls the AGC loop.

To rapidly reach the DC operating point, a fast mode is built into the three DC blocks.

### LO

The external VCO is AC-coupled at input LOIN. It is then buffered to drive the first mixer. LOIN also enters a quadrature divider-by-2, whose output signals are also buffered to drive the second mixers. The VCO frequency should be $^2/_3$ of the input RF signal.

The LO signal must be generated with an external frequency synthesizer and VCO or with a crystal oscillator.

## OPERATING MODES

To use the IC, all $V_{CC}$ pins must be connected to the supply voltage B++ (2.1 V). The 1.8 V regulated voltage sinks current from B++ and the 1.0 V regulated voltage from B+ (1.4 V). In a typical application, the B+ supply is the battery and the B++ supply is the DC/DC converter located in the baseband chip.

In normal operating mode, the receiver should be powered-on in fast mode. The fast mode can be turned off after several milliseconds.

Table 1 gives the definition of the polarity of the switching signals on the receive section.

**Table 1** Switching signals on the receiver

| SIGNAL | SECTION | LEVEL | ON/OFF |
|---|---|---|---|
| RXON | receive section powered-on | HIGH | on |
| | receive section powered-off | LOW | off |
| FASTON | fast mode powered-on | HIGH | on |
| | fast mode powered-off | LOW | off |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | – | 6 | V |
| ΔGND | difference in ground supply voltage applied between all grounds | note 1 | – | 0.3 | V |
| $P_{I(max)}$ | maximum power input | | – | 20 | dBm |
| $T_{j(max)}$ | maximum operating junction temperature | | – | 150 | °C |
| $P_{(max)}$ | maximum power dissipation | in stagnant air at 25 °C | – | 500 | mW |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |

### Note

1. Pins short circuited internally must be short circuited externally.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 90 | K/W |

## HANDLING

All pins withstand the ESD test in accordance with *“MIL-STD-883C class 2 (method 3015.5)”*.

## DC CHARACTERISTICS

$V_{CC}$ = 2.1 V; $T_{amb}$ = 25 °C; 930 MHz band application, 3% BER and 1600 bits/s 2 level; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Pins: $V_{CC(O)}$, DRV1, $V_{CC(FE)}$, $V_{CC(DC)}$, $V_{CC(LO)}$ and DRV2** | | | | | | |
| $V_{CC1}$ | supply voltage 1 (B++; see note 1) | over full temperature range | 1.85 | 2.1 | 3.3 | V |
| $V_{CC2}$ | supply voltage 2 (B+; see note 1) | over full temperature range | 1.05 | 1.4 | 1.5 | V |
| $I_{CC1(RX)}$ | supply current from B++ | RX section on; DC tested | | | | |
| | | $f_{RF}$ = 160 MHz | – | 2.4 | – | mA |
| | | $f_{RF}$ = 280 MHz | – | 2.4 | – | mA |
| | | $f_{RF}$ = 930 MHz | 2.35 | 2.7 | 3 | mA |
| $I_{CC2(RX)}$ | supply current from B+ | RX section on; DC tested | | | | |
| | | $f_{RF}$ = 160 MHz | – | 1.3 | – | mA |
| | | $f_{RF}$ = 280 MHz | – | 1.4 | – | mA |
| | | $f_{RF}$ = 930 MHz | 1.85 | 2.3 | 2.45 | mA |
| $I_{CC1(pd)}$ | standby current from B++ | Power-down mode; DC tested | 0 | 0.01 | 1 | μA |
| $I_{CC2(pd)}$ | standby current from B+ | Power-down mode; DC tested | 0 | 0.01 | 0.5 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Pins: RXON, FASTON, OUTI and OUTQ** | | | | | | |
| $V_{IH}$ | HIGH-level voltage | | $V_{CC}$ – 0.3 | $V_{CC}$ | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | LOW-level voltage | | –0.3 | – | +0.4 | V |
| $I_{IH}$ | HIGH-level static current | $V_{CC}$ – 0.4 V | –1 | – | +1 | µA |
| $I_{IL}$ | LOW-level static current | pin at 0.4 V | –1 | – | +1 | µA |
| **Pins: CAPI1A, CAPI1B, CAPQ1A and CAPQ1B** | | | | | | |
| $V_{CAP}$ | DC level | RX section on | 1.20 | 1.40 | 1.60 | V |
| **Pins: CAPI2A, CAPI2B, CAPQ2A, CAPQ2B** | | | | | | |
| $V_{CAP}$ | DC level | RX section on | 1.40 | 1.57 | 1.80 | V |
| **Pins: CAPI3A, CAPI3B, CAPQ3A, CAPQ3B** | | | | | | |
| $V_{CAP}$ | DC level | RX section on | 1.30 | 1.57 | 1.90 | V |
| **Pins: RFINA and RFINB** | | | | | | |
| $V_{RF}$ | DC level | RX section on | – | 0.92 | – | V |
| **Pins: IMOUTA and IMOUTB** | | | | | | |
| $V_{IMOUT}$ | DC level | RX section on | – | 0.17 | – | V |
| **Pins: $V_{CC(LO)}$** | | | | | | |
| $V_{Vcc(lo)}$ | DC level | RX section on | 0.95 | 1.00 | 1.05 | V |
| **Pins: $V_{CC(FE)}$** | | | | | | |
| $V_{Vcc(fe)}$ | DC level | RX section on | 1.75 | 1.80 | 1.85 | V |
| **Pins: FILOUTA and FILOUTB** | | | | | | |
| $V_{FILOUT}$ | DC level | RX section on | – | 0.24 | – | V |
| **Pins: AGCTAU and RSSI** | | | | | | |
| $V_{RSSI}$ | DC level | RX section on; FASTON is LOW<br>RX section on; FASTON is HIGH | –<br>$V_{CC}$ – 0.3 | 0<br>$V_{CC}$ | 0.30<br>– | V<br>V |
| $V_{AGCTAU}$ | DC level | RX section on; FASTON is HIGH | 1.50 | 1.60 | 1.70 | V |
| **Pins: GYROUTI and GYROUTQ** | | | | | | |
| $V_{GYROUT}$ | DC level | RX section on | 1.37 | 1.42 | 1.47 | V |
| **Output stage** | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $I_o$ = –5 µA | – | $V_{CC}$ – 0.2 | – | V |
| $V_{OL}$ | LOW-level output voltage | $I_o$ = 5 µA | – | 0.2 | – | V |

**Note**

1. For B+ and B++, see Fig.3.

## AC CHARACTERISTICS

$V_{CC}$ = 2.1 V; $T_{amb}$ = 25 °C; 930 MHz band application, 3% BER and 1600 bits/s 2 level; on evaluation board according to Fig.3; system measurement done using PCD5009, PCD5010 baseband; unless otherwise specified.

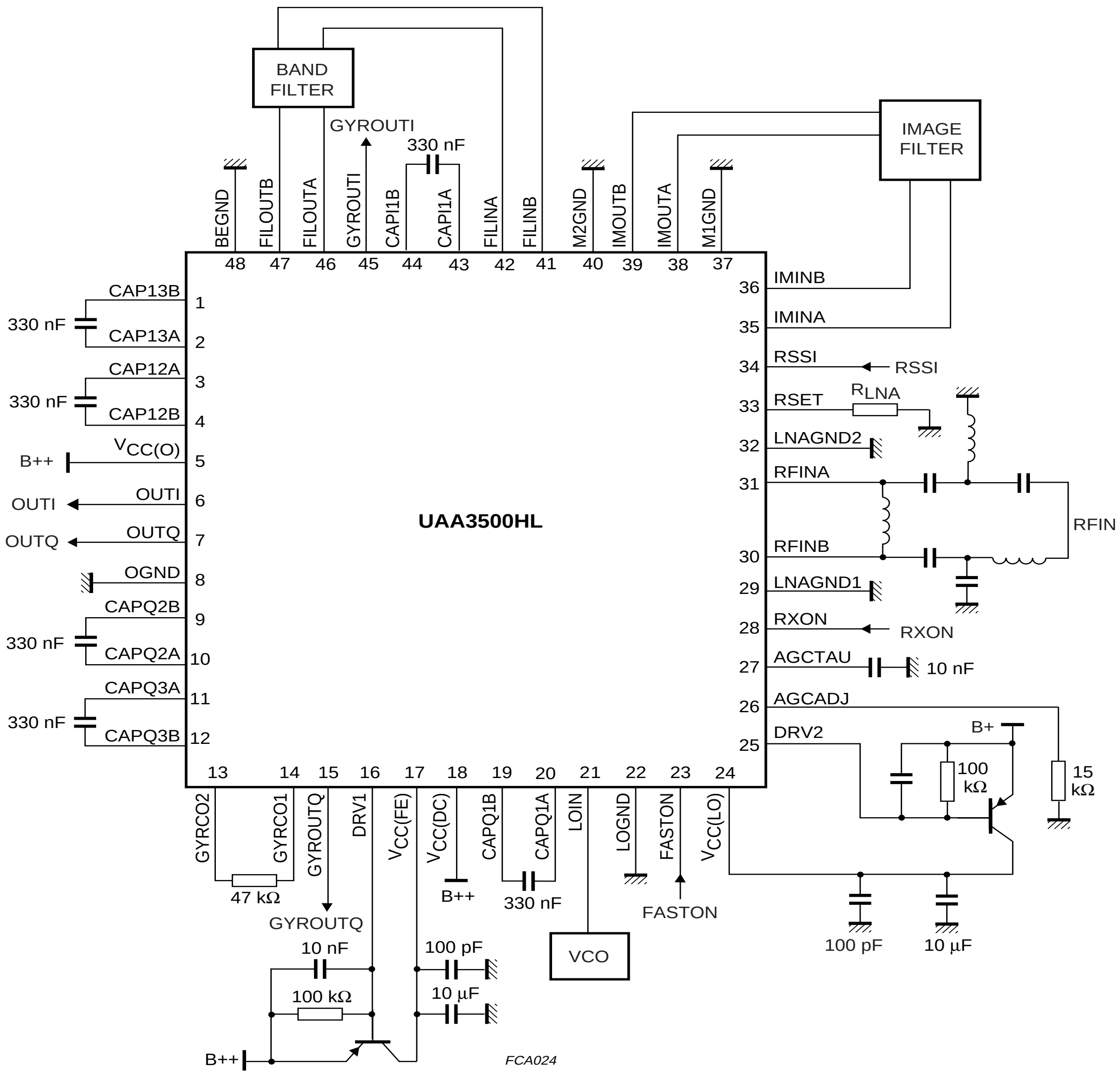
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Receiver** | | | | | | |
| $P_{i(ref)}$ | RF input sensitivity | 3% BER | | | | |
| | | $f_{RF}$ = 160 MHz; 1600 bits/s 2-level FSK | – | –128.5 | – | dBm |
| | | $f_{RF}$ = 280 MHz; 1600 bits/s 2-level FSK | – | –128 | – | dBm |
| | | $f_{RF}$ = 930 MHz; 6400 bits/s 2-level FSK | – | –126.5 | – | dBm |
| | | $f_{RF}$ = 930 MHz; 6400 bits/s 4-level FSK | – | –123 | – | dBm |
| $G_{(PCFE)}$ | front-end conversion power gain | from RF input to 2nd mixer input | | | | |
| | | $f_{RF}$ = 160 MHz | – | 20 | – | dB |
| | | $f_{RF}$ = 280 MHz | – | 12.8 | – | dB |
| | | $f_{RF}$ = 930 MHz | – | 12.7 | – | dB |
| $NF_{RX}$ | receiver noise figure | from RF input to 2nd mixer input | | | | |
| | | $f_{RF}$ = 160 MHz | – | 2.7 | – | dB |
| | | $f_{RF}$ = 280 MHz | – | 3.1 | – | dB |
| | | $f_{RF}$ = 930 MHz | – | 4.4 | – | dB |
| IP1 | 1 dB input compression point | from RF input to 2nd mixer input | – | –38 | – | dBm |
| IP2 | 2nd order intercept point | from 2nd mixer input to gyrator output | 45 | – | – | dBm |
| IP3 | 3rd order intercept point | from RF input to 2nd mixer input; note 1 | – | –33 | – | dBm |
| IM3 | 3rd order intermodulation | 3 signal measurement | 55 | – | – | dB |
| CCR | co-channel rejection | threshold +3 dB | – | 5 | – | dB |
| ACR | adjacent channel rejection | channel spacing = 25 kHz; from RF input to gyrator output | 65 | 70 | – | dB |
| $\alpha_{bl}$ | blocking immunity | frequency offset >1 MHz | 75 | 80 | – | dB |
| $G_{AGC}$ | front-end gain reduction by AGC step | | 7 | 8 | 9 | dB |
| $AGC_{th}$ | AGC threshold | above sensitivity | 20 | 25 | 30 | dB |
| $t_{on}$ | establishment time | until sensitivity +3 dB is reached | – | – | 30 | ms |
| ΔIQ | IQ channel unbalance | | – | – | 2 | dB |
| $R_{LNA}$ | LNA current set resistor | 160 MHz | – | 56 | – | kΩ |
| | | 280 MHz | – | 47 | – | kΩ |
| | | 930 MHz | – | 27 | – | kΩ |
| $R_{gyr}$ | gyrator cut-off frequency set resistor | cut-off frequency = 8.5 kHz | – | 47 | – | kΩ |
| **LO** | | | | | | |
| $f_{VCO}$ | VCO frequency | | – | $\frac{2}{3}f_{RF}$ | – | MHz |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **LNA** | | | | | | |
| $G_{LNA}$ | RF amplifier power gain | from RF input to image filter output | | | | |
| | | $f_{RF}$ = 160 MHz | – | 20 | – | dB |
| | | $f_{RF}$ = 280 MHz | – | 16.2 | – | dB |
| | | $f_{RF}$ = 930 MHz | 12.5 | 14.2 | – | dB |
| $NF_{LNA}$ | RF amplifier noise figure | from RF input to image filter output | | | | |
| | | $f_{RF}$ = 160 MHz | – | 1.8 | – | dB |
| | | $f_{RF}$ = 280 MHz | – | 1.9 | – | dB |
| | | $f_{RF}$ = 930 MHz | – | 2.2 | 2.5 | dB |
| $IP1_{LNA}$ | 1 dB input compression point | from RF input to image filter output | – | –27 | – | dBm |
| $IP3_{LNA}$ | 3rd order intercept point | from RF input to image filter output | –21 | –17.6 | – | dBm |
| **First mixer** | | | | | | |
| $G_{FM}$ | 1st mixer power gain | | –0.5 | 0 | – | dB |
| $NF_{FM}$ | 1st mixer noise figure | | – | 10.2 | 13 | dB |
| $IP1_{FM}$ | 1 dB input compression point | | – | –22 | – | dBm |
| $IP3_{FM}$ | 3rd order intercept point | | –12.5 | –11 | – | dBm |
| **Second mixer, PMA, Sallen-Key, 1st DC block and gyrator filter** | | | | | | |
| $Gv_{BE}$ | voltage gain | from 2nd mixer input to gyrator output | 42 | 45 | – | dB |
| $IP3_{BE}$ | 3rd order intercept point | from 2nd mixer input to gyrator output | – | –59 | – | dBm |
| **1st DC block** | | | | | | |
| $f_{cut\text{-}off}$ | cut-off frequency | measured at gyrator output; FASTON is LOW | – | 4 | – | Hz |
| $f_{cut\text{-}off}$ | cut-off frequency | measured at gyrator output; FASTON is HIGH | 150 | 400 | – | Hz |

**Note**

1. The two tones for intermodulation test would normally be set at 2 and 4 or 4 and 8 channels for type approval tests i.e 930 and 930.1 or 930.1 and 930.2 MHz.

## APPLICATION INFORMATION

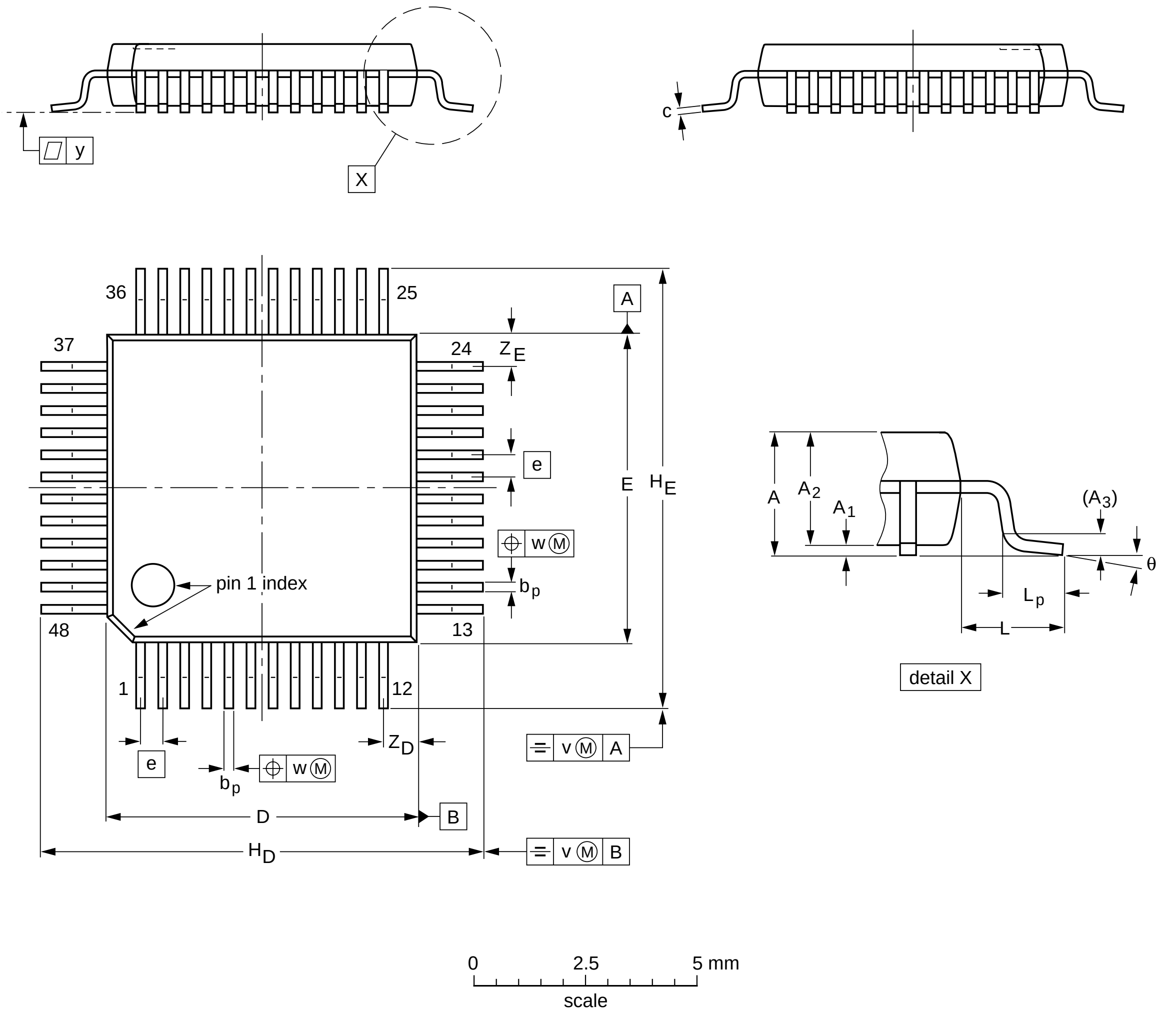



Electrical diagram of the UAA3500HL demonstration board for FLEX[TM] applications. All matching is to 50 Ω for measurement purposes.
B+ = 1.4 V; B++ = 2.1 V.

Fig.3 Demonstration board diagram.

## PACKAGE OUTLINE

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(1) | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D$(1) | $Z_E$(1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | 7°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT313-2 | | MS-026 | | | | ~~97-08-01~~<br>99-12-27 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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